Dr. Nisha Kuruvilla

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Academic Qualifications:

- **PhD inElectronics & Communication Engineering** from Center for Nanotechnology Research,VIT University Vellore for thesis title" Performance Analysis of Carbon Nanotubes for Futuristic IC Interconnects" in 2013
- **M Tech in Electrical Engineering with** Specialization in Microelectronics& VLSI from IIT Kanpur in 2002.
- **B Tech in Electronics Engineering** from Marathawada University in 1990.

Work Experience:

- 25 years and 6 months of Teaching Experience. (Both for UG and PG students)
- 1 year and 3 months of Industrial experience (HMT Kalamassery & Malayala Manorama)

Area of Interest

- Modeling and performance analysis of emerging devices in VLSI
- CNT Interconnects
- Low power VLSI designs
- VLSI Interconnects
- Digital VLSI

Publications

Papers published in referred International Journals	: **13Nos.**
Papers published in referred International Conference Proceedings	: **18 Nos.**
Papers published in referred National Conferences Proceedings	: **6 Nos.**

International Presentation

- Presented a paper in IEEEICM-2008 Conference at university of Sharja, UAE
- Presented a paper in IEEE ASP-DAC 2009 held at Pacifico Yokohama, Yokohama, Japan under the Emerging Technologies and Applications

Membership in Technical Organizations:

- IEEE member.
- MemberofIEEESSCS
- Life time Member of "The Indian Society for Technical Education (ISTE)" an organization for promoting the quality and standards in Technical Education.
- Member of the International Association of Computer Science and Information Technology (MIACSIT)

Subjects taught.

Subjects Taught: (UG Level)

- VLSI Design
- ASIC Design
- Solid State Electronics
- Digital Electronics
- Electronic Circuits
- Microprocessors
- Advanced Microprocessors
- Test and Measuring Instruments
- Linear integrated Circuits.

Subjects Taught: (PG Level)

- Electronic Design Automation Tools
- VLSI Design
- Low Power VLSI
- Physical Design Lab

Short Term Programs Coordinated

- National workshop on "Advanced Nano- Scale Device design Using TCAD" from 28/12/2015 to 01/01/2016 in association with IEEESSCS
- .IHRD FDP on " Semiconductor Devices, Circuits and Systems- with Research Perspective" from 04/07/2016 to 09/07/2016
- Two day workshop on "VLSI Design Automation" - 06/05/2016- 07/05/2016

AWARDS AND HONOUR

- ***Outstanding IEEE Student Branch Counselor International award*** for the academic year 2005-2006 by the Regional Activities Board and the Technical Activities Board of the IEEE.
- Recipient **Grurudarsanam Award 2014** by Sree Narayana Sevasamithi, in appreciation to the voluntary in engineering education.
- Coordinator of DST funded type-0 project worth 80 Lakh rupees in College of Engineering Chengannur.(2012-2017)
- *Recipient of international student fellowship* for participating and presenting paper in 14th Asia and South Pacific Design Automation Conference ASP-DAC 2009 held at Pacifico Yokohama, Yokohama, Japan under the Emerging Technologies and Applications topic.
- Reviewer of IEEE Design & Test of Computers magazine
- Reviewer of Journal of Circuits, Systems and Computers by World Scientific Publishing
- Received PhD degree in Nanoelectronics in 2013
- Won Best paper award in International conference on computing, communication and signal processing- 2016
- Won Best paper award in 2nd International Conference on Emerging Trends in Technology and Applied Science-2015

POSITONS HANDLED

- Principal, College of Engineering, Kallooppara, Pathanamthitta(2019 January to till date)
- Head of the Electronics Department of College of Engineering, Chengannur (May 2016 to May 2017), (2012 September-2014November), (2007-2010)
- Placement Officer of College of Engineering, Chengannur (2014 November to 2019 January), (2010 July to 2013 September)
- Member, Expert Visiting Committee, APJ Abdul Kalam Technological University

- Academic Auditor, APJ Abdul Kalam Technological University
- IEEE SSCS Branch Advisor (2014-till date) (founder advisor)
- PG Coordinator of College of Engineering, Chengannur (2010 June to 2012 June)
- IEEE WIE Kerala Section vice Chair(2010)
- IEEE Branch councilor (2004 June -2007 June)
- Cooperative Society Secretary of College of Engineering, Chengannur
- ISTE Chapter Secretary (1998-2000) (founder Secretary)

LIST OF FUNDED PROJECTS

- FIST Type 0 funded project from department of science and technology - worth 80 Lakh rupees in College of Engineering Chengannur.(2012-2017)

INTERNATIONAL REFERENCE

- The name and biography of Nisha has been selected for publishing in International Biography references **"Who is Who in world 2010 edition".**

INVITED TUTORIALS/LECTURES/CONFERENCE CHAIR

- "Emerging Trends in Device Technology" TKM Engineering College
- "Empowering Women in Technology" College of Engineering Adoor
- "Role of IEEE Wie in shaping professionalism", NIT Calicut
- "VLSI interconnects", IEEESSCS chapter SaintgitsEngg. College Chaper
- "The Role of CAD tools in research and teaching" , IETE FDP, SaintgitsEngg. College
- "Emerging Devices in VLSI " - LBS institute of technology for Women,.
- "Emerging technologies in VLSI", Bishop JerromInstitute , Kollam
- " Emerging VLSI interconnects" ,STTP College of Engineering, Karunagappaly
- " VLSI interconnects" at STTP on "Recent Trends in VLSI and MEMS" held at Government Engineering College, Barton Hill,Thiruvananthapuram
- "Low power VLSI" at ISTE STTP Government Model Engineering College, Ernakulam
- Chaired section on "Microelectronics" inInternational Conference held at Amal Jyothi College of Engineering, Kanjirappally
- Chaired section on National Conference held at Muslim Association College of Engineering, Venjaramoode, Trivandrum.
- Chaired section on "Microelectronics" at International Conference held at Government Engineering College (RIT-Kottayam)

LIST OF PUBLICATIONS

International Journal Papers

1. Anju Chakkikavil, Nisha Kuruvilla, Ayoob Khan, Shahul Hameed," Structural Optimization of Wavy FinFET for Leakage Reduction and Performance Enhancement", Advances in Science, Technology and Engineering Systems Journal Vol. 2, No. 3, 913-917 (2017)
2. Ravindran, A., George, A., Praveen, C. S., & Kuruvilla, N. (2017). Gate All Around Nanowire TFET with High ON/OFF Current Ratio. *Materials Today: Proceedings*, *4*(9), 10637–10642. https://doi.org/10.1016/j.matpr.2017.06.434
3. Nisha Kuruvilla and J. P. Raina. (2014*Impact* of *Bundle* Structure on Performance of on-Chip *CNT* Interconnects.Hindawi Publishing Corporation Journal of Nanotechnology Volume 2014, Article ID 217519, 8 pages).http://dx.doi.org/10.1155/2014/217519

4. Rahul Raj, Nisha Kuruvilla and Tintu K Thampi, "High Level Application Independent Optimum Voltage and Frequency Prediction for Low Power System" , International Journal of Computer Applications (0975 – 8887), pp 36-39, 2015
5. Jyothi A, Nisha Kuruvilla, Ayoob Khan and Shahul Hameed T A Impact of Fin Shape on Fin FET Performance, International Journal of Computer Applications (0975 – 8887) pp 1-4, 2015
6. Sarojini S Potti1 ,Dr.Sreelal S Pillai and Dr. Nisha Kuruvillla, "A Compact SPICE Model for Asymmetric Drain Spacer Extension FinFET"International Journal of ChemTech Research CODEN (USA): IJCRGG ISSN: 0974-4290 Vol.7, No.2, pp 842-849, 2014-2015
7. KollaramaSubramanyam , Nisha Kuruvilla and J. P. Raina.(2014), Physical Parameter Based Compact Expression for Propagation Constant of SWCNT InterconnectsWorld Academy of Science, Engineering and Technology, International Journal of Electrical, Electronic Science and Engineering Vol:8 No:1, pp139-143
8. AntuReeba Sam, Nisha Kuruvilla and J P Raina (2013), "Statistical Analysis of signal integrity issues in CNT interconnects due to contact resistance variations",International Journal of Scientific & Engineering Research,Volume 4, Issue 8, August 2013, ISSN 2229-5518
9. Nisha Kuruvilla, Kollarama Subramanyam and J. P. Raina. (2012). Physical Parameter Based Model for Characteristic Impedance of SWCNT Interconnects and its Performance Analysis. IISTE Journal of Innovative System Design and Engineering 3(9),16-26. (IC Impact factor- 6.94)
10. Nisha Kuruvilla, Amrutha S. R, J.P. Raina. (2012). Low-k Dielectric- A Potential Solution for Crosstalk Induced Signal Integrity issues in SWCNT Interconnects. *IOSR Journal of VLSI and Signal Processing, 1* (1), 29-32.
11. Nisha Kuruvilla, J P Raina, Arun Greig John and Athulya A, "Performance and Reliability Analysis of Bundled SWCNT as IC Interconnects", *Advanced Materials Research Vols. 129-131 (2010) pp 920-925,© (2010) Trans Tech Publications, Switzerland, doi:10.4028/www.scientific.net/AMR.129-131.920*
12. Nisha Kuruvilla, and J. P. Raina," Carbon Nanotubes – A Solution for Tera Hertz's IC Interconnect", International Journal of Recent Trends in Engineering (Electrical & Electronics), Vol. 1, No. 4, June 2009, pp 32-36
13. Arun Gerig John, Athulya A, ShnuGervasis, Akhil G. Nair and Nisha Kuruvilla, " A Performance Study of Carbon Nanotube Interconnects with CNT drivers: Comparison wit ITRS Predicted Drivers", International Journal of Scientific Computing, Vol.3 , No.1 , January- June 2009, pp 155-160.

International Conference Papers

1. C. Anju; Nisha Kuruvilla; T. E. Ayoob Khan; T. A. Shahul Hameed, "Performance Analysis of Wavy FinFET and Optimization for Leakage Reduction, 2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS) 2016, pp 83-88, DOI: 10.1109/iNIS.2016.030
2. Vani R and Nisha Kuruvilla ," 3D TCAD based parasitic capacitance extraction and frequency response analysis in multigate devices", International conference on computing, communication and signal processing, July 8th to 9th 2016, organized by College of engineering, Karunagappaly,pp 414-418 **(Won Best Paper Award)**
3. Anju C and Nisha Kuruvilla ," Optimized wavy FinFET- A solution for high performance low power device", International conference on computing, communication and signal processing, July 8th to 9th 2016, organized by College of engineering, Karunagappaly,pp 419-424

4. AntuReebaSam , Nisha Kuruvilla and Sarojini S Potti, "Compact Equivalent single conductor model for MWCNT Interconnect" , IEEESSCS sponsored 4th conference solid state circuits , 25th and 26th August 2016, pp170-175
5. Jyothi A, Nisha Kuruvilla, Ayoob Khan and Shahul Hameed T A Impact of Fin Shape on Fin FET Performance, 2ndInternational Conference on Emerging Trends in Technology and Applied Science, SAINTGITS College of Engineering, Kottayam, Kerala, India, 3oth April - 2d May 2015 **(Won Best Paper Award)**
6. Jesty Bhaskar and Nisha Kuruvilla, "Performance Analysis of Low Power Data Retentive Volatile Memory , 2nd International Conference on Emerging Trends in Technology and Applied Science, SAINTGITS College of Engineering, Kottayam, Kerala, India, 3oth April - 2d May 2015
7. Rahul Raj, Nisha Kuruvilla and Tintu K Thampi, "High Level Application Independent Optimum Voltage and Frequency Prediction for Low Power System" , 2 nd International Conference on Emerging Trends in Technology and Applied Science, SAINTGITS College of Engineering, Kottayam, Kerala, India, 3oth April -2nd May 2015
8. Sarojini S Potti1 , Dr. Sreelal S Pillai and Dr. Nisha Kuruvillla, "A Compact SPICE Model for Asymmetric Drain Spacer Extension FinFET", ICONN 2015 [4th -6th Feb 2015] International Conference on Nanoscience and Nanotechnology-2015 SRM University, Chennai, India
9. Nisha Kuruvilla, Anilkumar C V, "Performance Analysis of Carbon Nanotube Interconnects -A Statistical Approach", ICVLSI 2008, Feb. 14-16, 2008, pp 163- 168 , Organized by Velammal engineering College, Chennai.
10. Nisha Kuruvilla, Saju Thomas, Joseph John, "Studies on point to point optical wireless links", International conference on wireless communication networks, June 27-29, 2003, organized by SSN Engineering College, Chennai.
11. Nisha Kuruvilla, J P Raina and Arun Gerig John, "Performance and reliability analysis of Mixed CNT bundle vs SWCNT Bundle as IC Interconnects, International Conference on "Carbon Nanotechnology: Potential and Challenges", December 15-17, 2010, organized by Advanced Nanoengineering Materials Laboratory Department of Mechanical Engineering and Materials Science Programme Indian Institute of Technology Kanpur (IITK), Kanpur, (UP) India in association with Indian Society for Advancement of Materials and Process Engineering, pp 26-37
12. Nisha Kuruvilla and J.P.Raina, "Carbon Nanotube IC Interconnects of various geometries – A Performance Analysis", Poster present in International Symposium on nanotechnology Present &Future Trends, organized by Center of Nanotechnology research, VIT University, Vellore, August 25th&26th, 2010.
13. Nisha Kuruvilla, J P Raina, Arun Greig John and Athulya A, "Performance and Reliability Analysis of Bundled SWCNT as ICInterconnects", ICMMT 2010, September 17-19, 2010, Chongqing, China
14. Nisha Kuruvilla, J P Raina and Arun Gerig John, ""A Comparative Analysis of Process Fluctuations Induced Parasitic Variations of Mixed CNT vs SWCNT Bundle Interconnects", ICNB 2010,International Conference on Nanotechnology and Biosensors, Jan. 20-21, 2010, pp 12, Organized by IACQER
15. Nisha Kuruvilla and J.P.Raina "Statistical Sensitivity Analysis of Latency of Carbon Nanotube Interconnects due to Contact Resistance Variations", IEEE ICM 2008, 20th International Conference on Microelectronics December 14th -17th 2008, University of Sharjah. pp 340-343.
16. Nisha Kuruvilla and J.P.Raina "Performance Analysis of Carbon Chips", Poster present in 14th Asia and South Pacific Design Automation Conference ASP-DAC 2009, IEICE VLD Student Forum Poster Presentation, Jan. 19-22, 2009 at Pacifico Yokohama, Yokohama, Japan under the Emerging Technologies and Applications topic.

17. AntuReeba Sam, Nisha Kuruvilla and J P Raina “Statistical Analysis of signal integrity issues in CNT interconnects due to contact resistance variations”, ICGITS 2013, Saint Gits, Kottayam, 04.04.13-06.04.13
18. Tintu K Thampy, Nisha kuruvilla and Lisa Mathew,” An Optimized Architectural Level Leakage Aware Power Estimator using DVS”, ICCEECON2k15, Christ Knowledge City

National Conference Papers

1. Abdul Hakeem and Nisha Kuruvilla,” RF Parameter Extraction and Performance Analysis of Different Types of nanowire MOSFETs”, 3rd National Conference o he Emerging trends in VLSI, Embedded Systems, opto electronics and Signal Processing , organized by Model Engg. College , May 14-16 2015
2. Amrutha S R,Nisha Kuruvilla and J P Raina, ' Crosstalk Induced Signal Integrity Issues in various CNT Interconnect Geometries', *in the presentation of the 4th National Conference on Signal Processing, Communications and VLSI Design organized by Dept. ECE of Anna University of Technology, Coimbatore* on 9th june 2012.
3. Jain P Uthup and Nisha Kuruvilla “Performance Comparison of the logic devices using Silicon and CNT technology for deep submicron ICs” in the presentation of the 4th National Conference on Signal Processing, Communications and VLSI Design organized by Dept. ECE of Anna University of Technology, Coimbatore on 9th june 2012.
4. Nisha Kuruvilla, J.P. Raina. Anilkumar C V, ”Load Depended Performance Analysis of SWCNT as VLSI Interconnects”, National conference on VLSI and communication -2008 (NC-VCom 2008), Organized by SAINGITS College of Engineering, Mar 14th -15th , 2008 pp 141-144.
5. Nisha Kuruvilla, Liza Mathew, “Wire width planning for Zero Skew Routing in High Speed VLSI L Layouts”, National Conference on Microelectronics and Communication, SRM University, Tamil Nadu Aug. 24-27, 2007.
6. Nisha Kuruvilla, Joseph John, “Studies on IrDA Compatible Links for High Speed Indoor Data Transmission”, National Conference on Communication Networking (NCCN 2003), SRM Engineering College, Tamil Nadu Feb. 26-28, 2003